This listing of claims replaces all prior versions and listings of claims in the patent application.

Listing of Claims:

Claim 1. (currently amended) A demodulator for use in a satellite communication system, said demodulator operative for receiving a modulated signal having a data rate R, said modulated signal comprising retrievable data, said demodulator comprising:

means for partitioning said modulated signal into N ~~data channels~~shift registers, each of said ~~data channels~~shift registers having a data rate equal to R/N; and

means for processing the modulated signal contained in each of said N ~~data channels~~shift registers at a data rate of R/N, said means for processing operative for regenerating and outputting said retrievable data.

Claim 2. (currently amended) The demodulator of claim 1, wherein said means for partitioning said modulated signal into N ~~data channels~~shift registers comprises a demultiplexer, said demultiplexer operative for receiving samples of said modulated signal at a data rate R samples per second, and for outputting one of said received samples to one of said ~~data channels~~shift registers at a data rate of R/N samples per second.

Claim 3. (currently amended) The demodulator of claim 2, wherein said demultiplexer operates to output one of said received samples to each of said ~~data channels~~shift registers at a data rate of R/N samples per second.

Claim 4. (currently amended) The demodulator of claim 1, wherein said means for partitioning said modulated signal into N ~~data channels~~shift registers generates a clock signal having a rate of R/N, and said clock signal ~~be~~ is coupled to and utilized to clock the means for processing the modulated signal.

Claim 5. (original) The demodulator of claim 1, wherein said modulated signal is generated utilizing QPSK modulation.

Claim 6. (original) The demodulator of claim 1, wherein said data rate R is approximately 800MHz.

Claim 7. (original) A demodulator for use in a satellite communication system, said demodulator operative for receiving a modulated signal having a data rate R such that said demodulator receives R input samples per second, said modulated signal comprising retrievable data, said demodulator comprising:

a demultiplexer circuit having N shift registers, said demultiplexer circuit receiving said R samples per second as an input signal, said demultiplexer operative for inputting said R input samples sequentially into said N shift registers such that each of said shift registers receives input samples at a data rate of R/N samples per second; and

signal recovery circuitry for processing the input samples contained in each of said N shift registers so as to regenerate said retrievable data.

Claim 8. (original) The demodulator of claim 7, wherein said demultiplexer generates a clock signal having a rate of R/N, said clock signal be coupled to and utilized to clock the signal recovery circuitry for processing the modulated signal.

Claim 9. (original) The demodulator of claim 7, wherein said modulated signal is generated utilizing QPSK modulation.

Claim 10. (original) The demodulator of claim 7, wherein said data rate R is approximately 800MHz.

Claim 11. (currently amended) A method of demodulating an incoming modulation signal for use in a satellite communication system, said incoming modulation signal having a

data rate R, said modulation signal comprising retrievable data, said method comprising the steps of:

partitioning said modulation signal into N ~~data channels~~shift registers, each of said ~~data channels~~ shift registers having an input data rate equal to R/N;

processing the modulation signal contained in each of said N ~~data channels~~ shift registers at a data rate of R/N so as to regenerate said retrievable data; and

outputting said retrievable data.

Claim 12. (currently amended) The method of claim 11, wherein said step of partitioning said modulation signal into N ~~data channels~~ shift registers further comprises the step of outputting one of said received samples to one of said ~~data channels~~ shift registers at a data rate of R/N samples per second.

Claim 13. (currently amended) The method of claim ~~12~~11, wherein said step of partitioning said modulation signal into N ~~data channels~~ shift registers further comprises the step of outputting one of said received samples to each of said ~~data channels~~ shift registers at a data rate of R/N samples per second.

Claim 14. (currently amended) The method of claim 11, wherein said step of partitioning said modulation signal into N ~~data channels~~ shift registers further comprises generating a clock signal having a rate of R/N, said clock signal be coupled to and utilized in the step of processing the modulation signal.

Claim 15. (original) The method of claim 11, wherein said modulated signal is generated utilizing QPSK modulation.

Claim 16. (original) The method of claim 11, wherein said data rate R is approximately 800MHz.

Claim 17. (original) A method of demodulating an incoming modulation signal for use in a satellite communication system, said incoming modulation signal having a data rate R such that R input samples per second are received, said modulation signal comprising retrievable data, said method comprising the steps of:

demultiplexing the incoming modulation signal utilizing N shift registers, said demultiplexing step comprising inputting said R input samples sequentially into said N shift registers such that each of said shift registers receives input samples at a data rate of R/N samples per second; and

processing the input samples contained in each of said N shift registers utilizing signal recovery circuitry so as to regenerate said retrievable data.

Claim 18. (original) The method of claim 17, wherein said demultiplexing step comprises generating a clock signal having a rate of R/N, said clock signal being coupled to and utilized by said signal recovery circuitry.

Claim 19. (original) The method of claim 17, wherein said modulated signal is generated utilizing QPSK modulation.

Claim 20. (original) The method of claim 17, wherein said data rate R is approximately 800MHz.